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D. Remarks

Objections to Claims.

Claim 10 has been amended to address the stated grounds for objection.

Rejection of Claims 1-6, 8-13 and 15-20 Under 35 U.S.C. §102(e) based on *Yagishita et al.* (U.S. Patent No. 6,728,157).

The rejection of claims 1-6 will first be addressed.

The invention of claim 1 is directed to a memory device that includes at least a first memory cell array coupled to a read data and a separate write data bus. The at least first memory cell array accesses read data in response to a first type edge of a first clock and latches write data on at least the first type edge of the first clock. The memory device also includes at least a second memory cell array coupled to the read data bus and coupled to the write data bus. The at least second memory cell array accesses read data in response to a first type edge of a second clock and latches write data on at least the first type edge of the second clock. The second clock is phase shifted with respect to the first clock by less than 180°.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. The cited reference *Yagishita et al.* is not believed to show or suggest "accessing read data" and "latching write data on at least the first type edge of the second clock", as recited in claim 1.

Yagishita et al. discloses a "pseudo SRAM" semiconductor memory that includes multiple memory blocks (argued to correspond to Applicants' memory cell arrays). However, in *Yagishita et al.* a second memory block (BLK1) accesses read data and outputs write data in response to different signals, and not one "first type edge of the second clock", as recited in claim 1. This is shown in FIG. 4 of *Yagishita et al.*:

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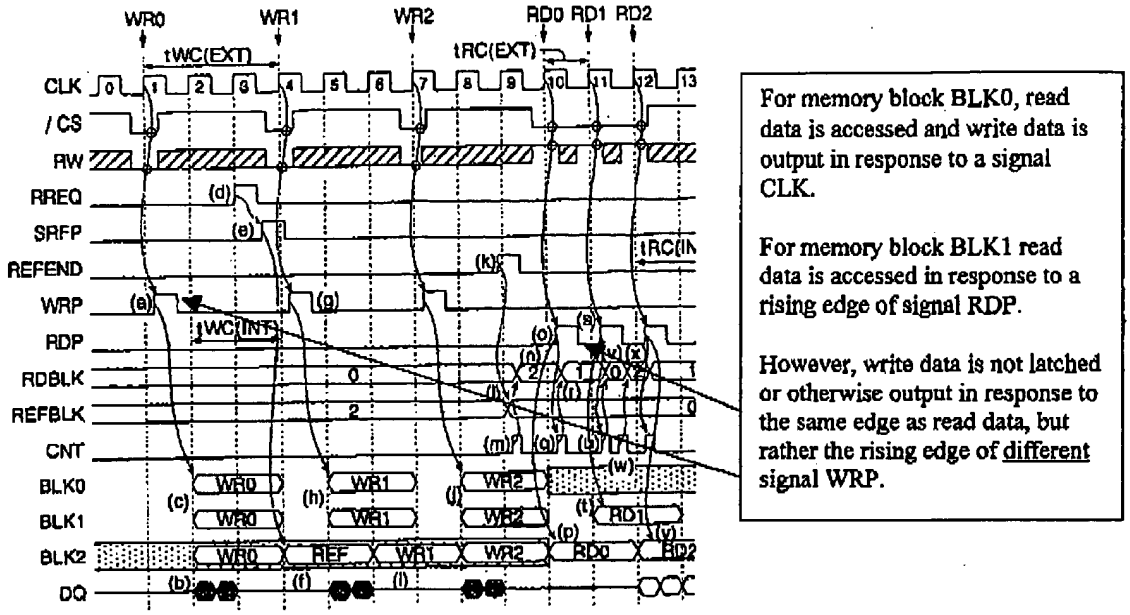

Fig. 4

Thus, because the reference shows read and write accesses to a second memory block in response to rising edges of different signals, the reference cannot show "accessing read data" and "latching write data in response to a second clock", as recited in claim 1.

Accordingly, because the cited reference does not show or suggest all the limitations of claim 1, this ground for rejection is traversed.

Various claims depending from claim 1 are believed to be separately patentable over the cited reference.

Claim 3, which depends from claim 1, recites that the first and second memory cell arrays comprise "static random access memory (SRAM) cells". The cited reference teaches the opposite, clearly indicating DRAM cells:

> The memory blocks BLK0-2 each have a plurality of memory cores ***each having DRAM memory cells***. (*Yagishita et al.*, Col. 6, Lines 22-23, emphasis added).

Thus, because Applicants' claim 3 recites SRAM cells and the reference teaches DRAM cells, all the limitations of claim 3 cannot be shown or suggested, and this claim is separately patentable over the cited reference.

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Claim 6, which depends from claim 1, recites that the memory device further includes an address bus, a first address latch, and a second address latch.

The semiconductor memory of *Yagishita et al.* clearly shows only one address latch not two address latches, as evidenced by FIG. 1 of the reference:

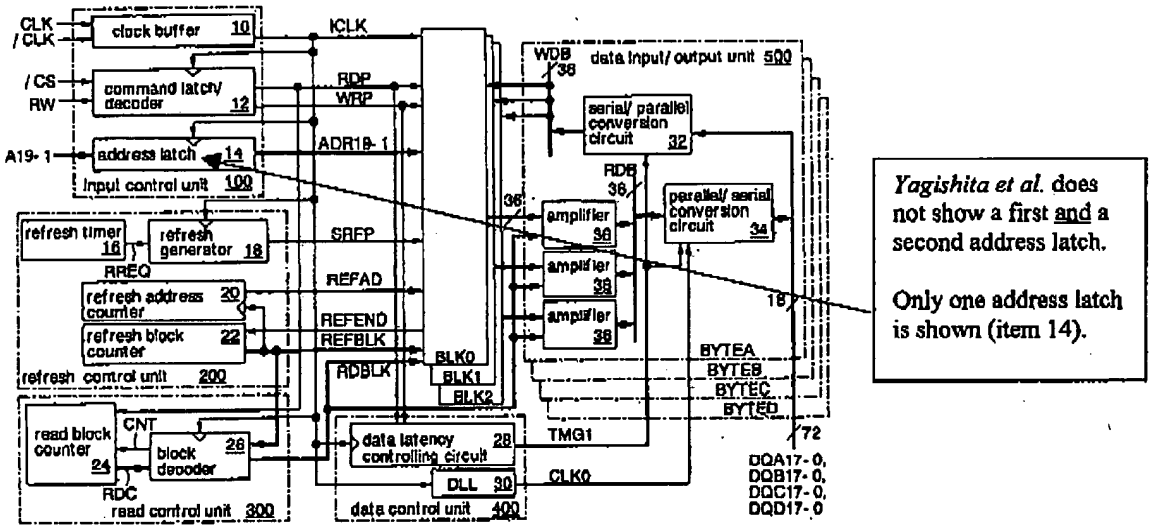

Fig. 1

Thus, because the reference only shows one address latch, all the limitations of claim 6 cannot be shown and are not believed to be suggested by the cited reference. Accordingly, claim 6 is also separately patentable over the cited reference.

Claim 8, which depends from claim 1, recites that the memory device further includes an address bus, a first write address decoder, a first write address register, a second write address decoder, and second write address register.

The limitations of claim 8 are not show in the reference. As understood from FIG. 1 of *Yagishita et al.*, the reference teaches only one decoder, and it is a ***command*** decoder (item 12) and not an address decoder. The reference argues a second write address decoder is shown in the reference:

> [Regarding claims 2-6, 9-13, Yagishita et al. discloses] ... a second write address decoder (Figure 2, 44)... (Office Action, dated 05/16/2005, Page 4, Lines 21-22).

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Applicants cannot agree with this reasoning. A reference to FIG. 2 of *Yagishita et al.* shows that item 44 is not an address decoder, but rather an address register:

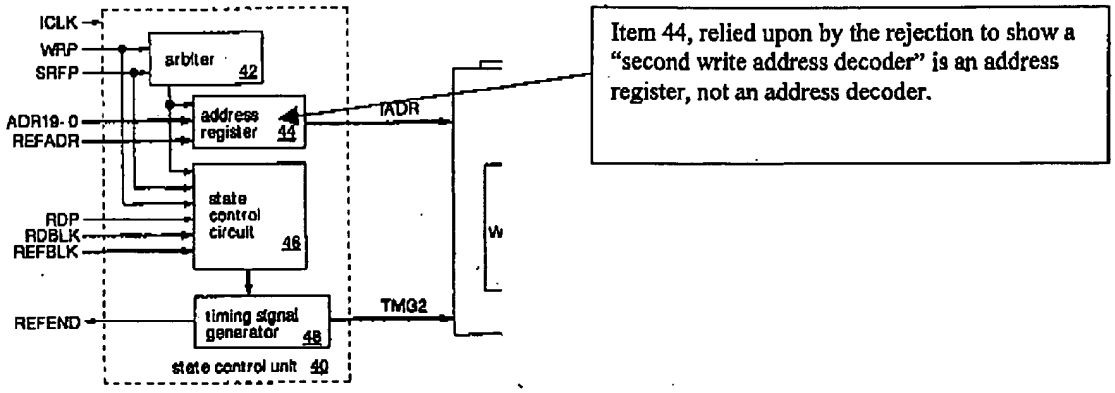

Fig. 2

Accordingly, Applicants do not believe the rejection has shown all the limitations of claim 8, and this ground for rejection is traversed.

The rejection of claims 9-13 will now be addressed.

The invention of claim 9 is directed to a memory device that includes a number of *N* memory cell arrays, each comprising at least two sections. The number *N* is an integer greater than 1. The memory device also includes a first write register that latches write data for a first of section of a first memory cell array on a rising edge of a first clock signal and latches write data for a second section of the first memory cell array on a falling edge of the first clock signal. In addition, the reference includes a second write register that latches write data for a first section of a second memory cell array on a rising edge of a second clock signal and latches write data for a second section of the second memory cell array on a falling edge of the second clock signal, the second clock signal have essentially the same frequency as the first clock signal but being phase shifted with respect to the first clock signal by about 180°/*N*.

Applicants note that a prima facie case of anticipation has not been established for this claim. While the rejection reasoning lists claim 9, the limitations of claim 9 are never discussed.[1] For this reason alone, this ground for rejection is traversed.

In addition or alternatively, Applicants note that while *Yagishita et al.* shows a write buffer (item WBUF in FIGS. 2 and 8 of *Yagishita et al.*), such buffers are never described as latching write data for different sections of memory cell arrays on falling edges of different clock signals, as recited in claim 9.

Accordingly, the reference does not show all the limitations of claim 9, and thus cannot anticipate this claim.

Claim 13, which depends from claim 9, recites "an address latch corresponding to each memory cell array". To address this ground for rejection, the comments set forth above for claim 6 are incorporated by reference herein. Namely, the reference shows only one address latch.

For all of these reasons, this ground for rejection is traversed.

The rejection of claims 15-20 will now be addressed.

The invention of claim 15 is directed to a method of increasing data throughput in a memory device. The method includes accessing a first of *N* memory cell arrays on a first-type edge and second-type edge of a first clock signal in response to one address value, accessing a second of the *N* memory cell arrays on a first-type edge and second-type edge of a second clock signal in response to the same address value. The second clock signal has essentially the same frequency as the first clock signal but is phase shifted with respect to the first clock signal by about 180°/*N*. The method also includes and outputting read data on a different bus than write data.

The cited reference *Yagishita et al.* does not show or suggest accessing different memory cell arrays in on edges of a first clock and a second clock. As shown by FIGS. 4 and 5 of the cited reference, operations are conducted based on one clock CLK. Various other signals are generated in response to such a clock, but none of these are phase shifted with respect to the first clock signal by about 180°/*N*.

[1] See the Office Action, dated 0516/2005, Page 4, starting at line 2. The rejection lists 9, but does not demonstrate where the limitations of claim 9 are shown in the reference.

Accordingly, because the reference does not show all of the limitations of claim 15, this ground for rejection is traversed.

Various claims depending from claim 15 are separately patentable over the cited reference.

Claim 16, which depends from claim 15, recites "latching read addresses on first-type edges of a first clock signal" and "latching write addresses on second-type edges of a first clock signal". In addition, the claim also recites "latching read addresses on first-type edges of a second clock signal" and "latching write addresses on second-type edges of a first clock signal". Such an arrangement is not shown or suggested by the cited reference.

Yagishita et al. does not show or suggest such an arrangement. First, as noted above, the reference does not show two different clock signals. Second, the latching of read addresses and write addresses on different type edges of such clock signals is never shown or described. The reference provides only one instance in which the latching of an address is described. This description does not distinguish between read and write addresses, and thus cannot show, and is not believed to suggest Applicants' claim 16 limitations:

> The address latch 14 receives address signals A19-1 in synchronization with the rising edges of internal clock signals ICLK, and outputs the received signals as internal address signals ADR19-1. (*Yagishita et al.*, Col. 5, Lines 10-13).

The above provides no teachings directed to the address latching arrangement recited in claim 16. Accordingly, claim 16 is believed to be separately patentable over the cited reference.

Claim 17, which depends from claim 15, recites a burst mode in which *M* sections are accessed from first and second memory cell arrays in response to different edges of a different clock signals. Such limitations cannot be shown by the reference. First, while the memory blocks of *Yagishita et al.* include a plurality of memory cores, such cores are never shown or suggested to be separately accessed. Second, a burst mode cannot be shown by the reference, as the word "burst" is never mentioned by the patent, as confirmed by a word search of the text, and absence of burst output data types.

Accordingly, this claim is also believed to be separately patentable over the cited art.

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Claim 20, which depends from claim 15, recites, in a write operation, "accessing the first of *N* memory cell arrays includes latching write data on first-type edges and second type edges of the first clock signal" and "accessing the memory cell array includes latching write data on first-type edges and second type edges of the second clock signal".

To address this ground for rejection Applicants incorporate by reference the same general comments set forth above for claim 9. In particular, the Examiner's burden cannot have been met and/or, at most, the cited reference shows a write buffer with no indication as to how, or even if, data is latched by such a buffer.

For all of these reasons, this ground for rejection is traversed.

Claims 10, 16-17 and 20 have been amended, not in response to the cited art, but to address a claim objection and typographical errors.

The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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